REMARKS

The Examiner is thanked for the thorough review and examination of this application. Claims 1-11 remain pending in this application. Claims 1, 3, 5, 7, and 10 have been amended as suggested by Examiner. Reconsideration of the application and the previous rejections are respectfully requested.

Claims 1-11 were tentatively rejected under 35 U.S.C. 112, second paragraph. Claims 1, 5, 7, and 10 were tentatively rejected under 35 U.S.C. 103(a) as allegedly unpatentable over Applicant's Admitted Prior Art (AAPA) in view of US 2004/0026741A1 to ***Saito***. Claim 3 was tentatively rejected under 35 U.S.C. 103(a) as allegedly unpatentable over AAPA in view of ***Saito*** and US 6,376,904 to ***Haba***. Claims 2, 6, 8, and 11 were tentatively rejected under 35 U.S.C. 103(a) as allegedly unpatentable over AAPA in view of ***Saito*** and US 6,118,310 to ***Esch***. Finally, claims 4 and 9 were rejected under 35 U.S.C. 103(a) as allegedly unpatentable over AAPA in view of ***Saito***, ***Haba***, and US 6,118,310 to ***Esch***.

35 U.S.C. 112 Rejections

Claims 2, 4, 6, 8, 9 and 11 stand rejected under 35 U.S.C. 112, second paragraph, as allegedly indefinite for failing to particularly point out and distinctly clam the subject matter which applicant regards as the invention. The Office Action contends that a meaning of the term "equivalent channel width" is not clear. The Office Action further suggests that the term "equivalent channel width" is interpreted as "channel width"

Applicant submits that the phrase "equivalent channel width" is different than the phjrase "channel width". According to page 4, lines 24-25 of specification, an equivalent width is composed of channel widths CH1 and CH2. In other words, the equivalent width is the sum of

the channel widths CH1 and CH2 in circuitry. Thus, the term "equivalent channel width" has been defined clearly and can not be amended to "channel width".

Claims 1, 3, 5, 7, and 10 were rejected under 35 U.S.C. § 112, second paragraph for the use of the term "equivalent" in the phrase "equivalent impedance." Applicant has amended these claims to remove the term "equivalent," as suggested by the Office Action.

Accordingly, Applicant respectfully submits that all claims 1-11 are now in full compliance with 35 U.S.C. § 112, second paragraph, and that all those corresponding rejections be withdrawn.

Claim Rejections

Claims 1 and 7 stand rejected under 35 U.S.C. 103(a) as allegedly unpatentable over AAPA in view of ***Saito***. Applicant respectfully traverses the rejection.

The Office Action contends that AAPA discloses most of the features of claims 1 and 7. However, the Office Action acknowledges that AAPA does not disclose ESD devices disposed on outermost sides of a connection area "having smaller impedance than other ESD protection devices," as recited in independent in claims 1 and 7. The Office Action contends that ***Saito*** discloses these features of claims 1 and 7 lacking in AAPA, and alleged that it would have been obvious to person of ordinary skill in the art at the time of invention to combine AAPA and ***Saito*** to achieve that invention of claims 1 and 7.

Applicant submits that ***Saito*** does not disclose or suggest ESD devices disposed on outermost sides of a connection area having smaller impedance than other ESD protection devices. ***Saito*** discloses a compensation of uneven resistances is disclosed. According Fig. 8

and paragraph [0037], resistances of protective elements are varied to provide equivalent resistances (including parasitic resistances).

As taught in the Abstract, *Saito* discloses, in a semiconductor integrated circuit device, an n-channel transistor area having an area A on a pad side and an area B on an internal circuit side. A plurality of protective elements are connected in parallel between a signal line and a power supply line. Each of the protective elements has resistors. Resistance of the resistors in the area A is set higher than resistance of the resistors in the area B by a value corresponding to resistance of parasitic resistance of the signal line included in the area A so that the resistance of the protective elements in the areas A and B are the same or almost the same as each other. A p-channel transistor area has the same configuration as that of the p-channel transistor area.

Moreover, according paragraph [0012] of *Saito*, the protective elements have the same or almost the same resistance as each other, and therefore the ESD load is evenly applied to the protective transistors.

In contrast to the teachings of *Saito*, claims 1 and 7 recite that impedances of the ESD protection devices ES_1 and ES_n are smaller than impedances of the other ESD protection devices ES_2 to ES_{n-1}. Claims 1 and 7 further recite that the ESD protection devices ES_1 to ES_n is configured corresponding to fan-out signal lines F_1 to F_n which extending from pads P_1 to P_n arranged sequentially. Thus, the ESD devices (ES_1 and ES_n) disposed on outermost sides of a connection area have smaller resistances than other ESD protection devices (ES_2 to ES_{n-1}). In contrast, the varied resistances of all protective elements in *Saito* are the same regardless of the positions of the protective elements to pads.

As demonstrated above, *Saito* discloses a compensation of uneven resistances, however, the varied resistances according to *Saito* are the same as each other. Thus, even if combined, the

combination of AAPA and *Saito* does not result in the invention of claims 1 and 7. For at least these reasons, claims 1 and 7 patently define over the cited art, and the rejections of claims 1 and 7 should be withdrawn.

Insofar as claim 1 is allowable, dependent claim 2 is also allowable. Likewise, insofar as claim 7 is allowable, dependent claims 8 and 9 are also allowable.

Claims 5 and 10 stand rejected under 35 U.S.C. 103(a) as allegedly unpatentable over AAPA in view of *Saito*. Applicant respectfully traverses the rejection.

Applicant respectfully disagrees for at least the reason that *Saito* does not disclose or suggest one of ESD devices having different impedance from other ESD protection devices.

Instead, *Saito* discloses a compensation of uneven resistances. According to Fig. 8 and paragraph [0037] of *Saito*, resistances of protective elements are varied to be the same. Moreover, according paragraph [0012], the protective elements have the same or almost the same resistance as each other, and therefore the ESD load is evenly applied to the protective transistors.

In contrast, claims 5 and 10 recite that the impedance of one ESD protection device is different from impedances of the other ESD protection devices. In contrast, the resistances of all protective elements in *Saito* are the same.

Further, and as demonstrated above, *Saito* also discloses a compensation of uneven resistances, however, the resistances areas according to *Saito* are the configured to be the same. Thus, the combination of AAPA and *Saito* does not result in the invention of claims 5 and 10. AAPA and *Saito* neither disclose nor suggest, singly or in combination, the invention of claims 5

and 10. Therefore, claims 5 and 10 patently defines over the cited art, and the rejections of claims 5 and 10 should be withdrawn.

Insofar as claim 5 is allowable, dependent claim 6 is also allowable. Insofar as claim 10 is allowable, dependent claim 11 is also allowable.

Claim 3 stands rejected under 35 U.S.C. 103(a) as allegedly unpatentable over AAPA in view of *Saito* and *Haba*. Applicant respectfully traverses the rejection. Neither *Saito* nor *Haba* teach, disclose, or suggest ESD protection devices having impedances gradually increasing from one outermost ESD protection device to some intermediate ESD protection device and decreasing from there to another outermost ESD protection device.

As noted above, *Saito* discloses a compensation of uneven resistances. According to Fig. 8 and paragraph [0037], resistances of protective elements are varied to be the same. Moreover, according paragraph [0012], the protective elements have the same or almost the same resistance as each other, and therefore the ESD load is evenly applied to the protective transistors.

In contrast, claim 3 recites that equivalent impedance of ESD protection devices ES_1 to ES_j gradually increase and those of ESD protection devices ES_{j+1} to ES_n gradually decrease. In other words, the impedance of the ESD protection devices decrease from the outermost ESD protection devices to the intermediate ESD protection devices. In contrast, *Saito* discloses a compensation of uneven resistances, however, the varied resistances according to *Saito* are the same as each other.

Moreover, according Fig. 4A of *Haba*, *Haba* only shows shapes of connections between the external terminals and die. Although these connections are configured as a fan-out form, ***Haba*** does not teach the relationship between the impedances of these connections. Thus, the

combination of AAPA, *Saito* , and *Haba* does not result in the invention of claim 3. AAPA, *Saito* , and *Haba* neither disclose or suggest, singly or in combination, the invention of claim 3.

Insofar as claim 3 is allowable, claim 4, depend from claim 3, including every claimed element thereof, is also allowable on its own merits in claiming additional elements not included in claim 3.

Conclusion

For the reasons as described above, Applicant believes that claims 1-11 are allowable in their present form. Withdrawal of the rejections and allowance of the claims are respectfully requested. Applicant has made every effort to place the present application in condition for allowance. It is therefore earnestly requested that the present application, as a whole, receive favorable consideration and that all of the claims be allowed in their present form.

No fee is believed to be due in connection with this Amendment and Response to Restriction Requirement. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

By: _____

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